IN THE CLAIMS

Please amend claim 10. Please add new claims 28-34. All pending claims and status indicators are set forth below. This listing of claims replaces all prior versions of the claims in the present application.

1-8. (Canceled).

9. (Previously Presented) A method for deterministic testing of edge-triggered logic, the method comprising:

setting a test signal in a test state so as to form a first scan chain that is responsive to a logic transition of a first clock signal and a second scan chain that is responsive to a logic transition of a second clock signal, the first and second scan chains each having an input for receiving scan data and an output for respectively providing the scan data; and

operating a third clock to control a latch interposed between the output of the first scan chain and the input of the second scan chain causing the latch to experience a hold state or a follow state, the hold state being experienced during a time period prior to the logic transition of the first clock signal and subsequent to the logic transition of the second clock signal such that data present at the output of the first scan chain prior to the logic transition of the first clock signal is held in the latch until after the logic transition of the second clock, the follow state being experienced outside the time period.

10. (Currently Amended) A circuit comprising:

a first clock domain comprising:

a first edge triggered memory device configured to receive a first data input signal, and configured to produce a first output signal in response to a first clock signal; ~~and~~

a first latch configured to receive the first output signal from the first edge triggered memory device and configured to produce a second output signal in response to a test clock signal;

combinatorial logic configured to receive each of a functional data signal and the second output signal from the first latch and configured to produce a combinatorial logic output signal; and

a multiplexor configured to receive each of the combinatorial output signal and a scan data input signal;

a second clock domain configured to receive the second output signal from the first clock domain and comprising:

a second edge triggered memory device configured to receive a second data input signal, and configured to produce a third output signal in response to a second clock signal; and

a second latch configured to receive the third output signal from the second edge triggered memory device and configured to produce a fourth output signal in response to the test clock signal.

11. (Previously Presented) The circuit, as set forth in claim 10, wherein each of the first edge triggered memory device and the second edge triggered memory device comprises a flip flop.

12. (Previously Presented) The circuit, as set forth in claim 10, wherein the first data input signal comprises one of a scan data input signal and a functional data input signal.

13. (Canceled)

14. (Previously Presented) The circuit, as set forth in claim 10, wherein the second clock domain is configured to receive the second output signal from the first latch at a multiplexor.

15. (Previously Presented) The circuit, as set forth in claim 10, comprising a third clock domain configured to receive the fourth output signal from the second latch.

16. (Previously Presented) The circuit, as set forth in claim 15, wherein the third clock domain comprises:

a multiplexor configured to receive the fourth output signal from the second latch;

a third edge triggered memory device configured to receive a third data input signal from the multiplexor, and configured to produce a fifth output signal in response to a third clock signal; and

combinatorial logic configured to receive each of a functional data signal and the fifth output signal from the third edge triggered device and configured to produce a combinatorial logic output signal, wherein the combinatorial output signal is delivered to the multiplexor.

17. (Previously Presented) The circuit, as set forth in claim 10, wherein the first latch is configured to produce the second output signal at approximately the same time as the second latch produces the fourth output signal.

18. (Previously Presented) A circuit comprising:

a plurality of clock domains, wherein each of the plurality of clock domains is coupled to another of the plurality of clock domains via a test path and is configured to receive a respective functional data signal and a respective clock signal and wherein each of the plurality of clock domains comprises:

a test clock input for receiving a test clock;

a test data input for receiving test data;

a test data output for producing output data; and

a test selection input for enabling a test mode; and

a plurality of inter-domain test latches arranged in the test path, wherein each of the plurality of inter-domain test latches is configured to pass data when the test clock is in a first state and configured to hold data when the test clock is in a second state.

19. (Previously Presented) The circuit, as set forth in claim 18, wherein each of the plurality of clock domains comprises a flip flop configured to receive the test data and configured to output the test data in response to the respective clock signals received at each of the plurality of domains.

20. (Previously Presented) The circuit, as set forth in claim 18, wherein each of the plurality of clock domains is configured to operate in the test mode when the test selection input is asserted and configured to operate in a functional mode when the test selection input is in a second state.

21. (Previously Presented) The circuit, as set forth in claim 18, wherein each of the plurality of clock domains comprises a multiplexor configured to receive the test selection input for enabling the test mode.

22. (Previously Presented) The circuit, as set forth in claim 18, wherein the plurality of clock domains comprises:

a first clock domain configured to receive a first clock signal;

a second clock domain configured to receive a second clock signal; and

a third clock domain configured to receive a third clock signal.

23. (Previously Presented) The circuit, as set forth in claim 18, wherein the plurality of inter-domain test latches are configured to connect each of the plurality of domains when the circuit is in the test mode.

24. (Previously Presented) The circuit, as set forth in claim 18, wherein each of the plurality of inter-domain test latches is configured to produce a respective output at approximately the same time when the test mode is enabled.

25. (Previously Presented) A method of testing a circuit comprising a plurality of clock domains each configured to receive a respective clock signal, wherein the circuit is configured to operate in a test mode when a test mode signal is asserted and

configured to operate in a functional mode when the test mode signal is de-asserted comprising:

executing a first shift cycle in the circuit, wherein executing the shift cycle comprises:

asserting a test mode signal, wherein assertion of the test mode signal configures a first edge-triggered device to receive test data from a test data input and configures each of a plurality of second edge-triggered devices in the system to receive data serially from a respective one of the first and the plurality of second edge-triggered devices;

de-asserting the respective clock signals to each of the respective clock domains;

simultaneously asserting each of the respective clock signals to shift the test data into the first edge-triggered device; and

de-asserting the test mode signal, such that the circuit operates in the functional mode; and

executing a sample cycle in the circuit, wherein executing the sample cycle comprises:

de-asserting each of the respective clock signals;

delivering test data to the first edge-triggered device;

de-asserting the test mode signal, thereby placing the circuit in the functional mode;

delivering test data to the first edge-triggered device and each of the plurality of second edge-triggered devices;

asserting the test clock to hold data on an output of each of the plurality of latches and at an input of each of the plurality of second edge-triggered devices; and

simultaneously asserting each of the respective clock signals.

26. (Previously Presented) The method, as set forth in claim 25, comprising executing a second shift cycle.

27. (Previously Presented) The method, as set forth in claim 26, wherein a scan data output produced during the first shift cycle is compared to a scan data output produced during the second shift cycle.

28. (New) A circuit comprising:

a first clock domain comprising:

a first edge triggered memory device configured to receive a first data input signal, and configured to produce a first output signal in response to a first clock signal; and

a first latch configured to receive the first output signal from the first edge triggered memory device and configured to produce a second output signal in response to a test clock signal;

a second clock domain configured to receive the second output signal from the first clock domain and comprising:

a second edge triggered memory device configured to receive a second data input signal, and configured to produce a third output signal in response to a second clock signal; and

a second latch configured to receive the third output signal from the second edge triggered memory device and configured to produce a fourth output signal in response to the test clock signal,

wherein the second clock domain is configured to receive the second output signal from the first latch at a multiplexor.

29. (New) The circuit, as set forth in claim 28, wherein each of the first edge triggered memory device and the second edge triggered memory device comprises a flip flop.

30. (New) The circuit, as set forth in claim 28, wherein the first data input signal comprises one of a scan data input signal and a functional data input signal.

31. (New) The circuit, as set forth in claim 28, wherein the first clock domain comprises:

combinatorial logic configured to receive each of a functional data signal and the second output signal from the first latch and configured to produce a combinatorial logic output signal; and

a multiplexor configured to receive each of the combinatorial output signal and a scan data input signal.

32. (New) The circuit, as set forth in claim 28, comprising a third clock domain configured to receive the fourth output signal from the second latch.

33. (New) The circuit, as set forth in claim 32, wherein the third clock domain comprises:

a multiplexor configured to receive the fourth output signal from the second latch;

a third edge triggered memory device configured to receive a third data input signal from the multiplexor, and configured to produce a fifth output signal in response to a third clock signal; and

combinatorial logic configured to receive each of a functional data signal and the fifth output signal from the third edge triggered device and configured to produce a

combinatorial logic output signal, wherein the combinatorial output signal is delivered to the multiplexor.

34. (New) The circuit, as set forth in claim 28, wherein the first latch is configured to produce the second output signal at approximately the same time as the second latch produces the fourth output signal.